Are Current SEE Test Procedures Adequate for Modern Devices and Electronics Technologies?

Kenneth A. LaBel
Co- Manager,
NASA Electronic Parts and Packaging (NEPP) Program
NASA/GSFC
ken.label@nasa.gov
301-286-9936
http://nepp.nasa.gov

Lewis M. Cohn, Defense Threat Reduction Agency
Ray Ladbury, NASA/GSFC

Outline of Presentation

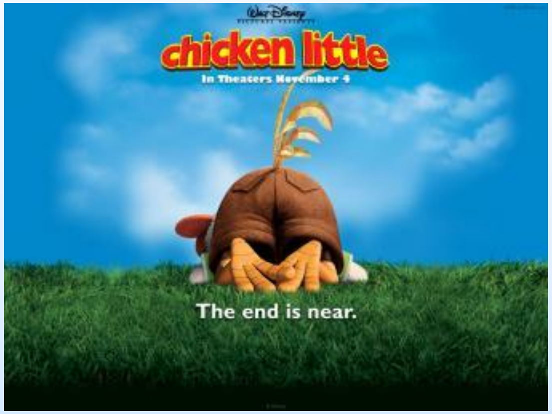
- Introduction and Background
- JEDEC Standard JESD57 – brief summary of related guidance
- Considerations for additions to test planning process
  - Beam-related characteristics
  - Test parameters
  - SEE Conditions
  - Data Capture
  - Destructive Events
- Discussion and Summary

Disclaimer:

This is not a comprehensive talk, but about considerations and thought processes

Introduction and Background

- At HEART 2007, we presented some of the burgeoning challenges associated with single event effect (SEE) testing of modern commercial memories
  - Package, device complexity, test fixture, and data analysis issues were discussed
  - "Complete" SEE Characterization would take 15years
  - Qualification test costs have a >4x increase over the last decade (up from 3X of last year)
- In this talk, we continue to explore the roles of technology with an emphasis on the existing SEE Test Procedures and some of the concerns related to modern devices
- The primary objective of the briefing is to provide some overarching guidance concerning the many considerations involved in the formulation of a SEE test plan provided in a "Checklist" format.
- We note that there is no such thing as a complete test check list and that the best approach is to develop a flexible test plan that takes into account the device type and functions, the device technology, circuit and package design, and, of course, test facility and beam characteristics



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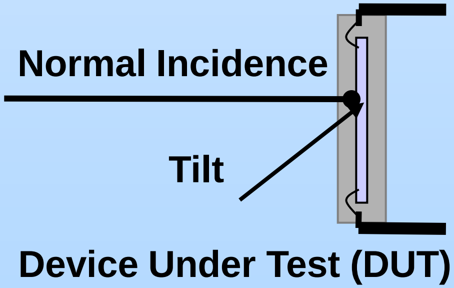
JESD57 – A Starting Point

- JEDEC JESD57 is the prime test standard utilized within the US for heavy ion SEE testing
  – Developed in the early and mid ’90s, it provides a reasonable starting base for planning SEE tests
- However, many new SEE-related considerations have forced us to consider some of the advice provided in JESD57. For example:
  - Section 3.1.2.1: “The beam angle is normally limited to a maximum of 60 degrees…’
    – This doesn’t require that you test to 60 degrees, just a recommended normal limit. Multiple results showing differing sensitivities at higher angles has made angular work a requirement for some technologies.
  - No discussion is present on asymmetric angular effects (i.e., tilting in both directions as well as changing the role of the device sample to the incident beam) stemming from technology and circuit layout

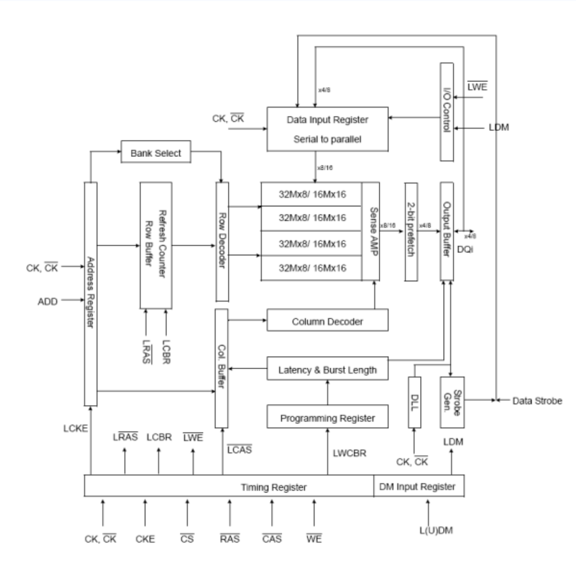


SEE Test Guidance

- **Given the rapidly changing nature of both technology and the related SEE issues being discovered, it would be nearly impossible to create up-to-date test standards in a timely fashion**
  - **The approach presented herein is to utilize a "checklist" in conjunction with SEE Test Standards for ensuring adequate radiation hardness assurance (RHA) is being met**
- **The following charts shall provide a look at selected checklist entries for digital electronics**
  - **We note that this is NOT an attempt at presenting a complete list given both the length of this talk and the rapid discovery of new "challenges"**
  - **But first, an example…**

Example: “Scrubbing” a Large Memory

- Modern state-of-the-art memories now have greater than 1 Gb worth of storage cells
- A typical dynamic test flow might look like
  - Write a test pattern to the entire device
  - Verify the pattern
  - Turn the beam on
  - Perform a read compare, capture/count error, correct error (read-modify write) for the address space
  - Repeat
- So what’s wrong with this picture?
  - Cycle time can be on the order of a minute for all address
    - Missed errors
    - Reverse bit-flips (i.e., flips back to correct state)
  - SEFIs can occur masking bit errors
  - All events are difficult to timetag when taking a minute to cycle through
    - Important for determining SEFI rates or MBUs
- Implication is that the particle flux rate must be very slow to avoid false data and improve data capture statistics



Commercial 1 Gb SDRAM

68 operating modes

operates to >500 MHz

Vdd 1.8V external, 1.25V internal

Beam-related Characteristics - 1

Category	*Test Consideration*	*Description*	*Rationale or Consideration*
SEU	**Energy dependence**	**Test with same effective LET with differing ions and energy**	**LET equivalence and cosine theta rule ineffective; increasing role of secondaries for scaled technologies for low LET & high energy particles; Increasing impact of charge sharing between critical UDSM IC nodes causing upsets in SEU “hard” devices**
SEE	**Ion Range**	**Ion range must be sufficient to reach sensitive volume/area at all test angles and ions used.**	**Bragg peak effects as well as metalization/package materials add uncertainties**
SEU	**Beam incidence**	**Vary tilt and roll (board rotate) to determine particle path MBU effects and cell symmetry; Angle range from perpendicular to grazing desirable**	**Transistors and cells are not symmetric and need to be irradiated at multiple angles; Test can be done at limited LETs for "calibration“; Increasing impact of charge sharing between critical scaled IC nodes causing upsets in SEU “hard” devices**

Beam-related Characteristics - 2

Category	Test Consideration	Description	Rationale or Consideration
SEU	Flux rate	Keeping the number of particles per second "tractable"	Caveat is to ensure particle interarrival time minimizes probability of two particles causing two events that look like MBU between event capture or that SEFIs don't mask other events.
SEE	Total dose dependence	TID can affect SEE response. Test matrix considers tracking TID levels.	If known, do not accumulate more than 80% of TID tolerance of device during SEE testing. If not known, monitor DUT for evidence of parametric degradation.
SEE	Displacement damage	Heavy-ion fluxes are usually too low to cause significant displacement damage. However, it can be a significant interference in proton testing.	If known, do not accumulate more than 80% of DD tolerance of device during SEE testing. If not known, monitor DUT for evidence of parametric degradation.

Test Set Parameters

Category	Test Consideration	Description	Rationale or Consideration
SEU	Temperature	Room temp - nominal; cryo is separate consideration	
SEU	Power supply voltage	Nominal; Nominal minus 5 to 10% (pending device type/specs)	
SEU	Memory or shift register test patterns	Various: all 0, all 1, checkerboard, inverse checkerboard, PRN	Determine worst-case and nominal SEU sensitivities of cell storage symmetry. Use worst-case where appropriate for majority of testing. Column and row striping may be required.
SEU	DSET Potential	Various operating speeds and voltage sensitivities: static, min, max, nominal, derated	Determine test required to look for propagation of transients to digital logic or cell. Includes clock frequency effects, operating voltage sensitivity and clock hits
SEU	Current monitoring	Strip charting of power supply(ies) current consumption required.	Resolution and frequency of measurement should be considered.
SEU	Operating modes	Devices can have high number of operating modes: try to determine a subset of interest for worst-case or use application-specific.	Data can vary from mode to mode, so be careful.

SEE Conditions - 1

Category	Test Consideration	Description	Rationale or Consideration
SEU	MBUs - general	Single particle, multiple cell events	Caveat is to ensure particle interarrival time minimizes probability of two particles causing two events that look like MBU between event capture Obtain physical to logical bit map for SRAM
SEU	Block errors	Page, column, row or partial errors of both	Must determine if recovery is possible without power cycle (mode register refresh, reload controls, reload, data,…). Real-time determination?
SEU	MBUs - angular	Vary tilt and roll (board rotate) to determine particle path MBU effects and cell symmetry; Angles from perpendicular to grazing desirable	Transistors and cells are not symmetric and need to be irradiated at multiple angles; Test can be done at limited LETs as "research"

SEE Conditions - 2

Category	*Test Consideration*	*Description*	*Rationale or Consideration*
SEU	**SEFI**	**Tests should take into account potential SEFIs that may manifest (control, test, or mode hit). This includes determining test fluences when events happen.**	**Determining of how to clear SEFI (re-write mode register, soft reset, power cycle, etc…) is important to determine. Real-time determination?**
SEE	**Stuck Bits**	**Need to determine if error is occurring at same location all the time. Re-writes and clears use.**	**If microdose, annealing can occur to remove event.**

Data Capture

Category	Test Consideration	Description	Rationale or Consideration
SEE	Statistics	Fluence levels should be high enough to get statistical significance of data without fear of beam pileup	Consider higher fluence level to look for small probability events such as in control logic.
SEE	Real-time error determination	Need to observe any non-traditional events	
SEFI	Current monitoring	Strip charting of power supply(ies) current consumption required.	Resolution and frequency of measurement should be considered. SEFIs sometimes show as a current draw change.
	Time-tagging	A requirement to look at single particle, multiple events or to post-process for block or SEFIs.	Caveat: For a memory array, all cells can be considered to have the same time tags during one read cycle of array. See also flux rate issues.

Destructive

Category	Test Consideration	Description	Rationale or Consideration
SEL	**Temperature**	**Worst-case for SEL is high-temp. 70-80C for COTS; 100-125C for Military**	**SEU data often taken at same time, but not required (i.e., biased device with functional check okay)**
SEL	**Power supply voltage**	**Nominal plus 5 or 10% (pending device type/specs)**	**Beware of confusing SEFI mode current changes with "non-destructive" SEL. Latent damage should also be considered. Also, ensure power rail is stiff and does not sag with increased current**
SEB/ SEGR	**Temperature**	**Data is *ambivalent* on high/low temp testing- matters for SEB & not for SEGR in general**	**Consider as part of SEL test using high temp, high Vdd**
SEGR/ SEB	**Ion Range**	**Ion range must be sufficient to reach sensitive volume/area for all ions used.**	**Bragg peak effects as well as metalization/package materials and depth of sensitive volume add uncertainties**

Destructive

Category	Test Consideration	Description	Rationale or Consideration
SEB/ SEGR	Power supply voltage	Vdd max or application plus 10%	Can also be a concern in non-power devices.
SEL	Current monitoring	Strip charting of power supply(ies) current consumption required.	Resolution and frequency of measurement should be considered.
SEL	Peak current	Stop beam when occurring. Current draw can increase with time.	Many SEL paths possible. Dwell tests can be considered. May not allow "runaway" levels if SEU performance data still needed.
SEL	Power cycling	Power supply should be incrementally lowered to determine holding voltage where SEL is removed.	SEL has been observed on < 1.25V devices.
Snapback	Mainly an issue in SEU hardened SOI NMOS	Snapback is a parasitic bipolar regenerative. Vdd is nominal +5/10%; WC temperature is high temperature.	Can be initiated by TID so need to ensure that this is not a factor. Current limiting can be considered.

Discussion and Summary

- Believe it or not, this has been a simplistic look at starting a checklist for SEE testing
  - Given a memory that has 68 operating modes, when a SEU occurs that changes the mode, just how do you determine what's going on?
    - Laser and microbeam tests can help, but not easily for modern packaged devices
- Expanding this approach to other more complex devices such as ADCs or processors as well as analog devices should be considered
- The recommendation is to use the existing test standards as a starting point
  - Just make your own checklist for the device/technology/issues being considered